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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/830,068	04/23/2004	Young Joon Ahn	YHK-0135	7680

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EXAMINER	
DONG, DALEI	
ART UNIT	**PAPER NUMBER**
2879	

DATE MAILED: 05/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EV

Office Action Summary	Application No.	Applicant(s)	
	10/830,068	AHN, YOUNG JOON	
	Examiner	Art Unit	
	Dalei Dong	2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. P2003-26401, filed on April 25, 2003.

Specification

2. The disclosure is objected to because of the following informalities:

In paragraph 14, line 2, "the environment of 200~300", should read the environment of 200°C ~ 300°C.

Appropriate correction is required.

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: PLASMA DISPLAY PANEL HAVING BUFFER LAYER BETWEEN THE SEALING LAYER AND THE SUBSTRATE AND METHOD OF FABRICATING THE SAME.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 3, 5, 10, 11, 15-17, 19 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,514,111 to Ebihara.

Regarding to claim 1, Ebihara discloses in Figures 1 and 5A-C, a plasma display panel (1), comprising: a first substrate (2); a second substrate (7) facing the first substrate (2) with a discharge space therebetween; a sealing layer (12 or 320) located between the first substrate (2) and the second substrate (7); and a buffer layer (4 or 240) formed between the first substrate (2) and the sealing layer (12 or 320) to compensate the thermal stress of the first substrate (2) and the sealing layer (320) (see column 5, lines 35-47).

Regarding to claim 3, Ebihara discloses in Figures 1 and 5A-C, the buffer layer (4 or 240) is formed by a low-melting-point glass paste mainly comprising lead oxide (see column 4, lines 27-38) and the first substrate (2) is made of glass which is a different material from that of the buffer layer and thus a range of thermal expansion coefficient of the buffer layer is different from a range of thermal expansion coefficient of the first substrate.

Regarding to claim 5, albeit, Ebihara discloses the buffer layer and the sealing layer both comprises mainly of PbO, however, Ebihara specifically discloses the buffer layer having a softening point of 580°C (see column 6, lines 41-53) and the sealing layer

having a softening point of 400°C (see column 7, lines 37-48) and thus, the buffer layer and the sealing layer may comprises of the same material however with different component compositions. Therefore, a range of thermal expansion coefficient of the buffer layer is different from a range of thermal expansion coefficient of the sealing layer.

Regarding to claim 10, Ebihara discloses in Figures 1 and 5A-C, a protective film (6) formed on the first substrate (2) where the buffer layer (4 or 240) has been formed.

Regarding to claim 11, Ebihara discloses in Figures 1 and 2A-C, an upper dielectric layer (25) formed on the first substrate (22); and a protective film (26) formed on the upper dielectric layer (25).

Regarding to claim 15, Ebihara discloses in Figures 2A-C and 5A-C, a fabricating method of a plasma display panel, comprising the steps of: forming a buffer layer (24) on a first substrate (22); and forming a sealing layer (32) on the buffer layer (24) (see column 6, line 34 to column 7, line 53 and see column 8, line 49 to column 9, line 25).

Regarding to claim 16, Ebihara discloses in Figures 2A-C and 5A-C, providing a second substrate (27) facing the first substrate (22) where the sealing layers (32) has been formed; and joining the first substrate (22) with the second substrate (27) (see column 6, line 34 to column 7, line 53 and see column 8, line 49 to column 9, line 25).

Regarding to claim 17, Ebihara disclose in Figures 2A-C, forming an upper dielectric layer (25) on the first substrate (22); forming a protective film (26) on the upper dielectric layer (25) (see column 6, line 34 to column 7, line 53).

Regarding to claim 19, Ebihara discloses in Figures 1 and 5A-C, the buffer layer (4 or 240) is formed by a low-melting-point glass paste mainly comprising lead oxide (see column 4, lines 27-38) and the first substrate (2) is made of glass which is a different material from that of the buffer layer and thus a range of thermal expansion coefficient of the buffer layer is different from a range of thermal expansion coefficient of the first substrate.

Regarding to claim 21, albeit, Ebihara discloses the buffer layer and the sealing layer both comprises mainly of PbO, however, Ebihara specifically discloses the buffer layer having a softening point of 580°C (see column 6, lines 41-53) and the sealing layer having a softening point of 400°C (see column 7, lines 37-48) and thus, buffer layer and the sealing layer may comprises of the same material however with different component composition. Therefore, a range of thermal expansion coefficient of the buffer layer is different from a range of thermal expansion coefficient of the sealing layer.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2, 7-9, 18, and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,514,111 to Ebihara in view of U.S. Patent No. 6,097,149 to Miyaji.

Regarding to claim 2, Ebihara discloses in Figures 1 and 5A-C, a plasma display panel (1), comprising: a first substrate (2); a second substrate (7) facing the first substrate (2) with a discharge space therebetween; a sealing layer (12 or 320) located between the first substrate (2) and the second substrate (7); and a buffer layer (4 or 240) formed between the first substrate (2) and the sealing layer (12 or 320) to compensate the thermal stress of the first substrate (2) and the sealing layer (320) (see column 5, lines 35-47).

Ebihara further discloses the buffer or dielectric layer (24) is formed by a low-melting-point glass paste mainly comprising PbO (see column 4, lines 27-38).

However, Ebihara does not specifically disclose the detailed composition of the dielectric layer as claimed.

The Miyaji reference teaches in Figures 1-5, a plasma display panel having a buffer layer (18) composed of PbO, B_2O_3, Al_2O_3 and SiO_2 (see column 7, lines 25-47) for

the purpose of effectively forming a stable dielectric layer when different materials are used for forming bus electrodes in the plasma display panel.

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have utilize the buffer layer of Miyaji for the plasma display panel of Ebihara in order to effectively form a stable dielectric layer when different materials are used to form the bus electrodes in the plasma display panel. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art.

Regarding to claim 7, the thermal expansion coefficient of the first substrate is merely a property of the material used in manufacture the first substrate, and the property of the material does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations and thus this limitation has not given patentable weight.

Regarding to claim 8, the thermal expansion coefficient of the sealing layer is merely a property of the material used in manufacture the sealing layer, and the property of the material does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations and thus this limitation has not given patentable weight.

Regarding to claim 9, the thermal expansion coefficient of the buffer layer is merely a property of the material used in manufacture the buffer layer, and the property of the material does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations and thus this limitation has not given patentable weight.

Regarding to claim 18, Miyaji teaches in Figures 1-5, a plasma display panel having a buffer layer (18) composed of PbO, B_2O_3, Al_2O_3 and SiO_2 (see column 7, lines 25-47) and it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art and the motivation to combine is the same as above.

Regarding to claim 23, the thermal expansion coefficient of the first substrate is merely a property of the material used in manufacture the first substrate, and the property of the material does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations and thus this limitation has not given patentable weight.

Regarding to claim 24, the thermal expansion coefficient of the sealing layer is merely a property of the material used in manufacture the sealing layer, and the property of the material does not differentiate the claimed apparatus from a prior art apparatus

satisfying the claimed structural limitations and thus this limitation has not given patentable weight.

Regarding to claim 25, the thermal expansion coefficient of the buffer layer is merely a property of the material used in manufacture the buffer layer, and the property of the material does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations and thus this limitation has not given patentable weight.

8. Claims 4, 6, 20 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,514,111 to Ebihara in view of U.S. Patent No. 6,495,262 to Igeta.

Regarding to claim 4, Ebihara discloses in Figures 1 and 5A-C, a plasma display panel (1), comprising: a first substrate (2); a second substrate (7) facing the first substrate (2) with a discharge space therebetween; a sealing layer (12 or 320) located between the first substrate (2) and the second substrate (7); and a buffer layer (4 or 240) formed between the first substrate (2) and the sealing layer (12 or 320) to compensate the thermal stress of the first substrate (2) and the sealing layer (320) (see column 5, lines 35-47).

However, Ebihara does not disclose the thermal expansion coefficient of the buffer layer is the same as the thermal expansion coefficient of the first substrate.

The Igeta reference teaches in Figures 1, a display panel, comprising: a buffer layer (2B) having thermal expansion coefficient same as thermal expansion coefficient of

the first substrate (1B) (see column 8, line 60 to column 9, line 3) for the purpose of alleviating and absorbing the strain stresses between the first and second substrate during cooling and furthermore providing a hermetically sealed case which can stay stably airtight after it has been sealed off.

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have utilize the buffer layer having same thermal expansion coefficient as of the first substrate of Igeta for the plasma display panel of Ebihara in order to alleviate and absorb the strain stressed between the first and second substrate during cooling and furthermore provide a hermetically sealed case which can stay stably airtight after it has been sealed off.

Regarding to claim 6, Igeta teaches in Figure 3, the thermal expansion coefficient of the buffer layer (22b) is the same as the thermal expansion coefficient of the sealing layer (22a) and the motivation to combine is the same as above.

Regarding to claim 20, Igeta teaches in Figure 1, the thermal expansion coefficient of the buffer layer (2B) is the same as the thermal expansion coefficient of the first substrate (1B) and the motivation to combine is the same as above.

Regarding to claim 22, Igeta teaches in Figure 3, the thermal expansion coefficient of the buffer layer (22b) is the same as the thermal expansion coefficient of the sealing layer (22a) and the motivation to combine is the same as above.

9. Claims 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,514,111 to Ebihara in view of U.S. Patent No. 6,261,144 to Nishiki.

Regarding to claim 12, Ebihara discloses in Figures 1 and 5A-C, a plasma display panel (1), comprising: a first substrate (2); a second substrate (7) facing the first substrate (2) with a discharge space therebetween; a sealing layer (12 or 320) located between the first substrate (2) and the second substrate (7); and a buffer layer (4 or 240) formed between the first substrate (2) and the sealing layer (12 or 320) to compensate the thermal stress of the first substrate (2) and the sealing layer (320) (see column 5, lines 35-47); and an upper dielectric layer (25) formed on the first substrate (22); and a protective film (26) formed on the upper dielectric layer (25).

However, Ebihara does not disclose the buffer layer is formed to be extended from the upper dielectric layer.

The Nishiki reference teaches in Figure 7A, a plasma display panel having an upper dielectric layer (18) formed on the first substrate (14) and the buffer layer is formed to be extended from the upper dielectric layer (18) for the purpose of efficiently sealing of the plasma display panel.

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have utilize the buffer layer extended from the upper dielectric layer of Nishiki for the plasma display panel of Ebihara in order to efficiently seal the plasma display panel.

Regarding to claim 13, Ebihara discloses the buffer layer (24) is separately formed of a different material from the upper dielectric layer (25) (see column 6, lines 34-65).

Regarding to claim 14, Nishiki discloses the buffer layer (17) and the upper dielectric layer (18) are formed of the same material (see column 9, lines 39-51) and the motivation to combine is the same as above.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following prior art are cited to further show the state of the art of composition of a plasma display panel.

U.S. Patent No. 5,336,121 to Baret.

U.S. Patent No. 6,218,777 to Jones.

U.S. Patent No. 6,414,434 to Nakano.

U.S. Patent No. 6,605,834 to Lee.

U.S. Patent No. 6,614,412 to Hirano.

U.S. Patent No. 6,827,623 to Nakatake.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dalei Dong whose telephone number is (571)272-2370. The examiner can normally be reached on 8 A.M. to 5 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimeshkumar Patel can be reached on (571)272-2457. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

D.D.
May 3, 2005

Joseph Williams
Primary Examiner
Art Unit 2879